ArchSem: Formalising concurrent CPU architectures to support verification in Rocq

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https://github.com/rems-project/archsem

Context: My trajectory

Started by building a toy OS in 3rd year: Fun but full of bugs

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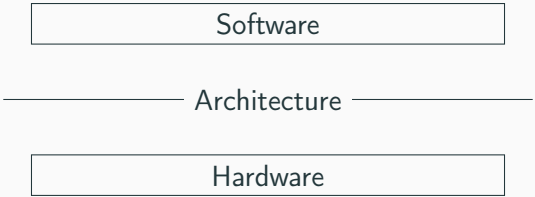
Need good architecture models

What is an architectural model



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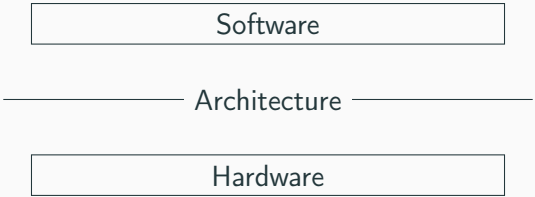

More concretely:

Defines an envelope of allowed behaviours:

- Set of final states from an initial state
- Allowed executions traces/witness

Why we need one

Better architecture specifications

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Architecture proofs

- Verification Morello (CHERI-Arm)
- Morello-Cerise (PLDI25)
- Virtual memory (VM) refinement

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System software verification

- SeKVM
- NOVA (BlueRock, WIP)
- AWS Nitro
- WIP: pKVM (in Android since 14)

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arm intel RISC-V

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- Verification of an CHERIoT-Ibex Processor (JasperGold, 2025)
- Intel's microcode verification (ACL2)
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seL4 CertiKOS

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Compiler verification

- CompCert
- CakeML
- ...

How: Decomposing the architecture

ISA model

Architecture pseudo-code: ASL, Sail, ...

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Memory model

ISA model $\rightarrow$ Machine model

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For compiler/application verification:

- Plain arithmetic
- Plain memory
- Optionally mixed-size accesses
- Register dependencies tracking

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~~**Memory model**~~ **Concurrency model**

ISA model $\rightarrow$ Machine model

User

For compiler/application verification:

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System

For system/runtime verification:

- Relaxed configuration registers
- Virtual memory, MMU, TLB
- Instruction fetching (icaches)
- Exception and Interrupts

ISA models

`0b100011111000011` $\Longrightarrow$ `ADD R1, R2, R3` $\Longrightarrow$ `R1 = R2 + R3`

ISA models (Alasdair Armstrong, Brian Campbell, ...)

`0b100011111000011` ⟹ `ADD R1, R2, R3` ⟹ `R1 = R2 + R3`

arm

ASL
(316 kLoC)

⇓


Sail
(433 kLoC)

RISC-V®


Sail
(22 kLoC)

intel

ACL2
(Not official)

⇓


Sail
(30 kLoC)

Concurrency models

MP+dmb.sy+ctrl AArch64

Initial state: 0:X2=y; 0:X1=x; 0:X0=1; 1:X3=x; 1:X1=y; 1:X0=0; 1:X2=0; y=0; x=0;	
Thread 0	Thread 1

STR X0,[X1]//a
DMB SY//b
STR X0,[X2]//c
	LDR X0,[X1]//d
	CBNZ X0,LC00
	LC00:
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Allowed: 1:X0=1; 1:X2=0;	

(a) Litmus test source

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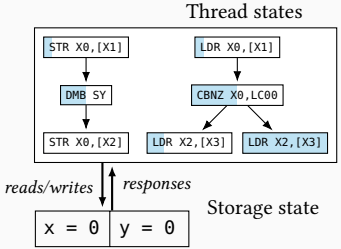

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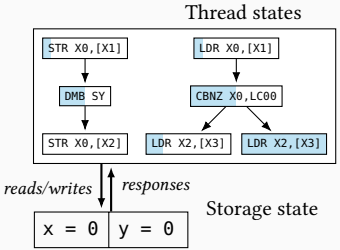

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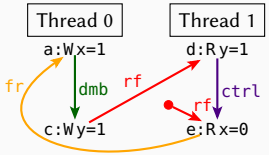

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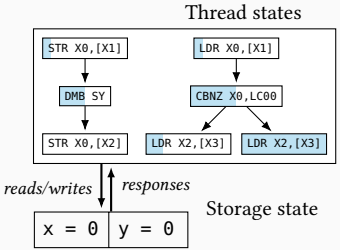

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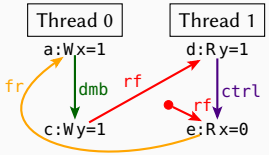

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Increasingly complex: Need full formalisation

Previous work

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- Architecture models containing full ISA model
- In an ITP, not just a test oracle (e.g. Herd or Isla)
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	Toy or simplified ISA	Real-ISA
Test oracle	Herd(current)	Isla, RMEM, Herd(WIP)
ITP	Promising (POPL 19), IMM's Arm, ...	ArchSem

ArchSem

A reusable formal framework to formally define CPU architecture models

Requirements

- Architecture generic
- Concurrency model generic (Axiomatic, Promising, micro-architectural, ...)
- ISA model generic
- Executable
- Usable for proof

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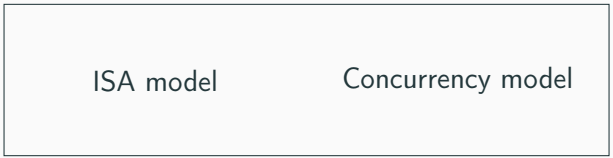

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Generic Interface

Arch Instantiation

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ISA in Sail
Armv9.4 ISA
RISC-V ISA
TinyArm ISA
TinyX86 ISA

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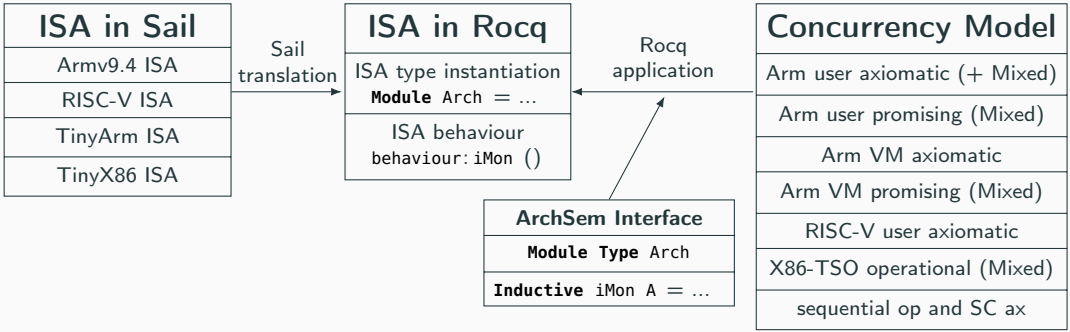
Concurrency Model
Arm user axiomatic (+ Mixed)
Arm user promising (Mixed)
Arm VM axiomatic
Arm VM promising (Mixed)
RISC-V user axiomatic
X86-TSO operational (Mixed)
sequential op and SC ax

Organisation



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| RegWrite (r: reg) (val : bv 64) (* () *)
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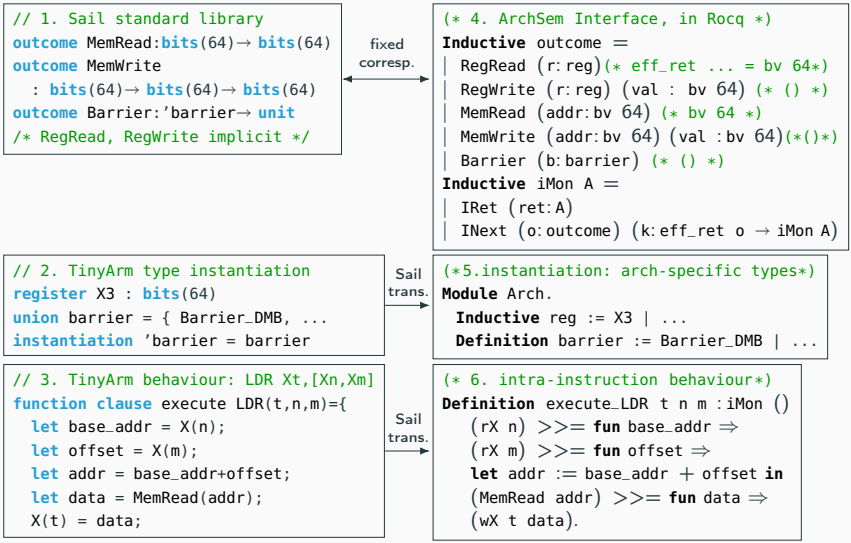
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(* 6. intra-instruction behaviour*)
Definition execute_LDR t n m : iMon ()
(rX n) >>= fun base_addr ⇒
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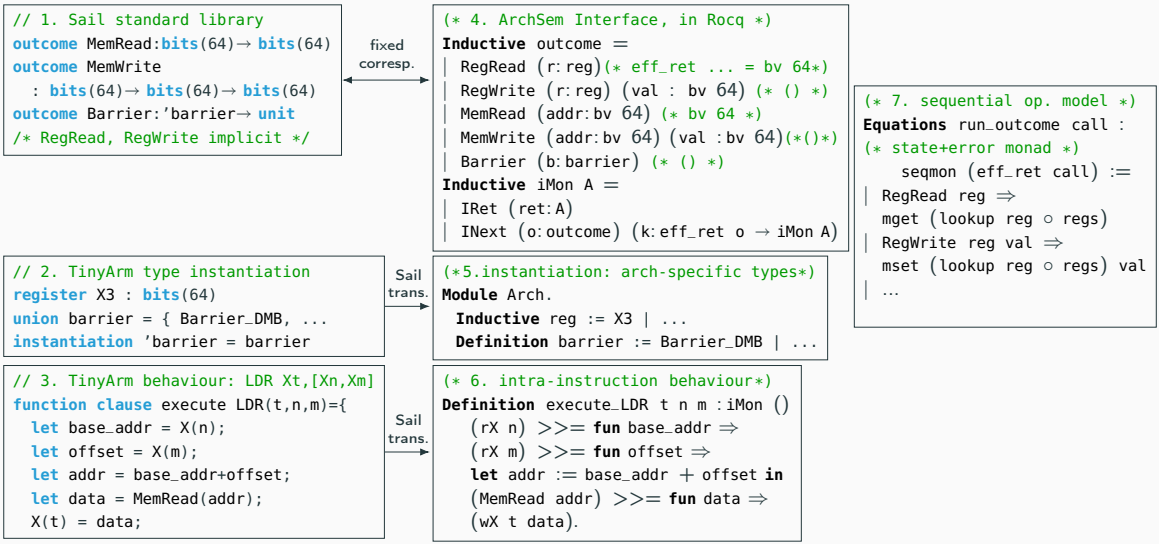
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```
(* 8. LDR concrete trace*)
(*as in axiomatic models*)
[RegRead X3 &↦ 0x100;
 RegRead X4 &↦ 0x1000;
 MemRead 0x1100 &↦ 0x2a;
 RegWrite X7 0x2a &↦ ()]
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Let's run a simple instruction on a sequential model

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LDR X1, [X0]
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                addr = R0;
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Practical example

Let's run a simple instruction on a sequential model

	`addr = R0;`	`addr ← RegRead R0;`
`LDR X1, [X0]`	`val = MemRead(addr);`	`val ← MemRead 8 addr Exp;`
	`R1 = val;`	`RegWrite R1 val`

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Sequential model

$$
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\texttt{R0} &\mapsto \texttt{0x42} \\
\texttt{R1} &\mapsto 0 \\
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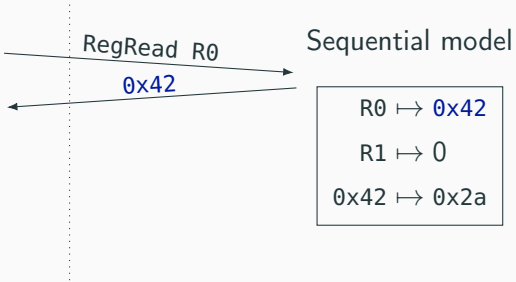

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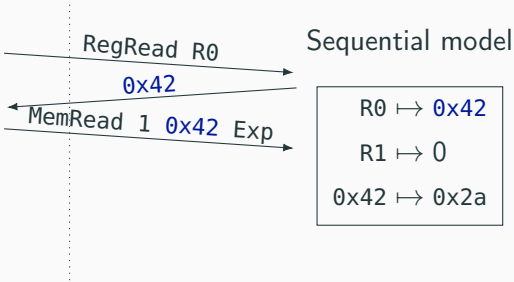

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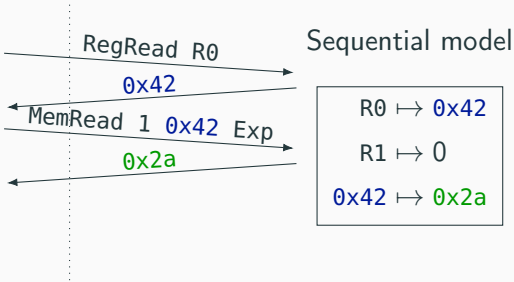

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LDR X1, [X0]    val = MemRead(addr);
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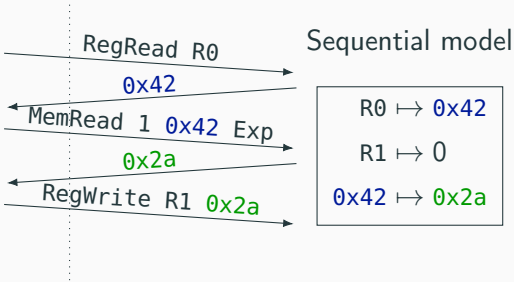

Practical example

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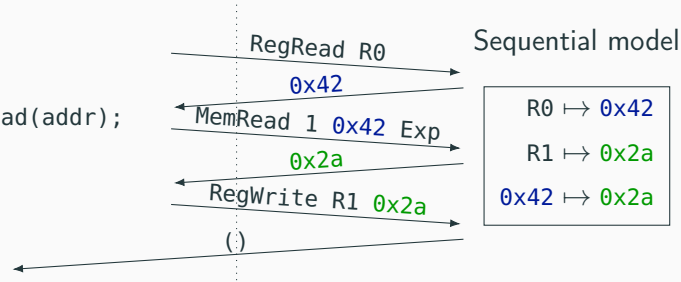

ISA models as free monads

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Allows decomposing reasoning between ISA and concurrency

Concurrency model implementation

Axiomatic models

- Use intra-instruction trace
- Stitch into candidate executions
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VM Promising model (with Yeji Han)

Update/improvement of the ESOP 2022 model by Ben Simner et al.

- Each memory access preceded by a translation (with some corresponding views)
- Maximal operational TLB model: Cache everything that is allowed to be cached.
- Add TLB Invalidate (TLBI) instructions to the main memory trace
- Relaxed system register history per-thread.
- Managed translation failure faults and returns

We found many behaviours implicitly allowed by axiomatic model that shouldn't have been

What can we do with this?

Proving architecture properties

Model equivalence

Sanity checks e.g.
seq $\Longleftrightarrow$ SC ax on single thread
(Nils Lauermann)

Model refinement

e.g. VM to UM abstraction theorem

Reasoning about programs

AxSL

Reasoning about axiomatic weak memory model with load buffering

Open: Systems program logic

What kind of ressources to represent CPU components:

- Page tables
- Incoherent caches
- Interrupts

VM Theorem – cartoon (with Thomas Baureiss)

Theorem (VM abstraction – very cartoon version)

The armv9-A architecture can be configured to provide a sound illusion of virtual memory.

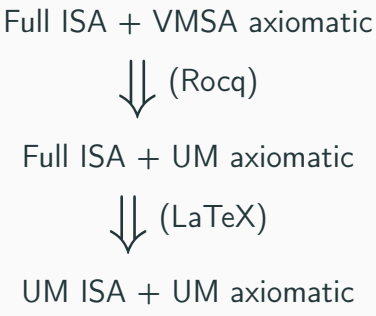
Theorem (VM abstraction – cartoon version)

In any armv9-A machine state at EL0 with a simple Stage 1 page-table configuration that doesn't map the page-tables themselves, any EL0 execution allowed by the VMSA model (full ISA + VMSA axiomatic) is also allowed by the User model (ISA without translation + User axiomatic).

VM Theorem – sketch

First: Isabelle ISA-only proof

Then:



AxSL

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TOPLAS (extension of POPL24 paper)

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HT-MICRO-MEMREAD-RDEP-EXT

$$\left\{ \begin{array}{l} (1)\mathrm{NoLocalWrites}(x) * (2)d = (\mathrm{dom}(regs), \emptyset) * \\ (3)\mathrm{PoPred}(e_{\mathrm{po}}) * (4)\mathrm{CtrlPreds}(srcs_{\mathrm{ctrl}}) * \\ (5) \mathop{\Large *}_{(r \mapsto v@E) \in regs} r \overset{\mathrm{r}}{\mapsto} v@E * (6) \mathop{\Large *}_{(e_{\mathrm{lob}} \mapsto P_{\mathrm{lob}}) \in m} (e \rightsquigarrow P_{\mathrm{lob}}) * \\ \forall e, v, e_w. \left(\begin{array}{l} (7)\mathrm{GraphFacts}(e, os, vr, x, v, e_w, e_{\mathrm{po}}, srcs_{\mathrm{ctrl}}, d, regs) \mathrel{-\!\!*} \\ ((8)\mathrm{Lob}(\mathrm{dom}(m), e) * (9)\mathrm{Flow}_{\Phi}(e, x, v, e_w, m, P)) \end{array} \right) \end{array} \right\}$$

MemRead *os vr x d*

$$\left\{ v, E. \begin{array}{l} \exists e, e_w.\, E = \{e\} * (10)\mathrm{NoLocalWrites}(x) * (11)\mathrm{PoPred}(e) * (12)\mathrm{CtrlPreds}(srcs_{\mathrm{ctrl}}) * \\ (13) \mathop{\Large *}_{(r \mapsto v@E) \in regs} r \overset{\mathrm{r}}{\mapsto} v@E * (14)\mathrm{GraphFacts}(e, os, vr, x, v, e_w, e_{\mathrm{po}}, srcs_{\mathrm{ctrl}}, d, regs) * \\ (15) e \rightsquigarrow P(x, v, e_w) \end{array} \right\}_{tid,\Phi}$$

How to use this to prove systems code?

- 95% of the code is standard imperative sequential code
  - We sort of know how to deal with that (maybe not to full scale)

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- 95% of the code is standard imperative sequential code
  - We sort of know how to deal with that (maybe not to full scale)
- 5% interact with hardware features and weak memory concurrency
  - That the part we don't know how to do well

Future work and Conclusion

- Proof structure questions:
  - For the 95%: we can use a simplified but sound model then prove refinement

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    - Building a logic on low-level layer and stacks of logical abstractions

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- Proof structure questions:
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    - Building stacks of model refinement
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- Partiality (Handling UB)
- Intra-instruction parallelism
- Full test campaign against the state of the art
- More models
- More proofs relating models
- Lean?

Thank you for your attention!

Why multiple styles of models

Axiomatic models

Naturally too relaxed:

- Need explicit constraints
- Easy to allow unwanted behaviours

Operational models

Naturally too strict:

- More relaxed $\Longrightarrow$ More complexity

Writing in both styles helps identify unconsidered cases,.

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"Bugs" we found by trying to operationalize models

- Read commit problems for mixed-size axiomatic Arm vs Flat
- TLB ordering questions, discovered when making Promising Arm for VMSA

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- "Easy" with acyclicity of `(p)po` $\cup$ `rf` (c.f. GenMC)
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Speculation vs Completion

Plan and paper math but no implementation

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| Async : iMon A → (unit → iMon (future A))
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Affected instructions

CAS, CSEL, LDP, STP, any unaligned access, 95% of SIMD load and stores